Development of the Readout Controller for KASINICS

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ABSTRACT

Korea Astronomy and Space Science Institute (KASI) is developing the KASI Near Infrared Camera System (KASINICS) which will be installed on the 61 cm telescope at the Sobaeksan Optical Astronomy Observatory (SOAO) in Korea. KASINICS is equipped with a ALADDIN III Quadrant (512×512 InSb array, manufactured by Raytheon). For this instrument, we make a new IR array control electronics system. The controller consists of DSP, Bias, Clock, and Video boards which are installed on a VME bus system. The DSP board includes TMS320C6713, FPGA, and 384MB SDRAM. Clock patterns are downloaded from a PC and stored on the FPGA. USB 2.0 is used for the communication with the PC and UART for the serial communication with peripherals. Each of two video boards has 4 video channels. The Bias board provides 16 voltage sources and the Clock board has 15 clock channels. Our goal of readout speed is 10 frames sec^{-1}. We have successfully finished operational tests of the controller using a 256×256 ROIC (CRC744). We are now upgrading the system for the ALADDIN III array. We plan to operate KASINICS by the end of 2006.

Keywords: near infrared, infrared camera, IR array controller

1. INTRODUCTION

The Space Astronomy Group of the Korea Astronomy and Space Science Institute (KASI) is developing the KASI Near Infrared Camera System (KASINICS) which will be installed on a ground-based telescope (61 cm Ritchey-Chretien type) at the Sobaeksan Optical Astronomy Observatory (SOAO). We use the 512×512 InSb array (ALADDIN III Quadrant, Raytheon Co.) for observations in J, H, Ks, and L-bands. The optics of the KASINICS was designed to remove unwanted thermal radiations from the optical telescope using an Offner system. The weight including a cooler and a controller box is about 80 kg. The cold box of the camera is cooled down to 80 K. The detector housing is cooled down to 30 K and maintains the temperature within ±0.1 K. More details of the optical and mechanical parts are described in "KASINICS: KASI Near-Infrared Camera System" by Cha et al.[1] in this proceedings.

Although we could use ready made controller like a SDSU III (Leach et al., 2003)[2], we developed a new controller for many kinds of electronic test and other applications. The Controller mainly consists of DSP board, Clock board, Bias board, and Video board. We can also control and monitor the temperature and the vacuum status, and the filter wheel with PC via RS232C communication. In this paper, we introduce the properties of each board and the result of initial test.

2. ELECTRONICS OVERVIEW

The KASINICS readout controller has a DSP (digital signal processor) board for the main control, Bias and Clock boards for the infrared (IR) array readout, and two Video boards for digitizing the image signals. Power, data and command signal lines of each board are connected to the standard VME bus backplane. One Video board has 4 signals

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process chain. We can process more than four output-signals with additional Video boards. The Bias board provides 16 bias voltages and the Clock board supply 15 clocking channels. Also the Bias and Clock boards can be added like the Video boards. Fig. 1 shows the block diagram of the KASINICS electronics and Fig. 2 is a picture of the controller box connected to the power supply.

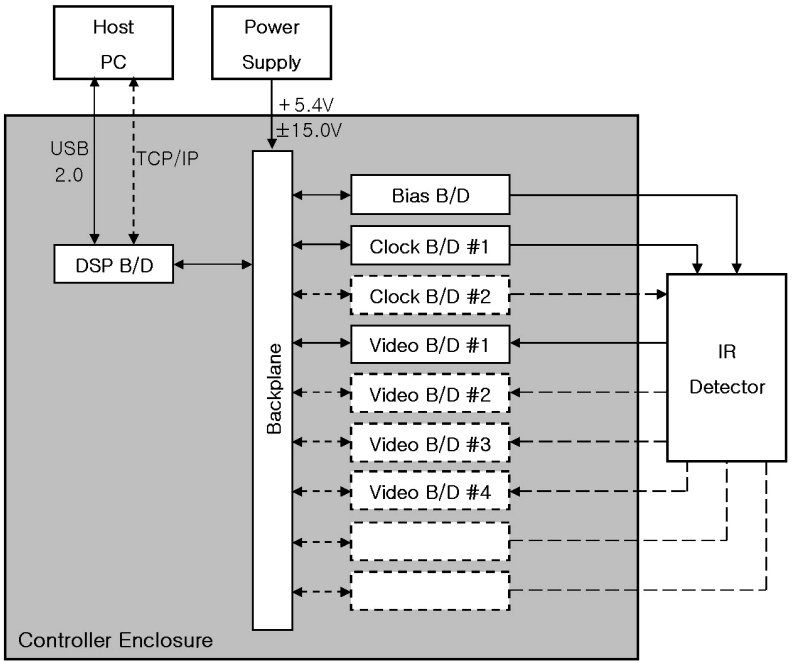

Figure 1. Block diagram of the KASINICS controller. The DSP, Bias, Clock, and Video boards are mounted on a standard VME bus backplane. The controller can be extended with up to 10 circuit boards.

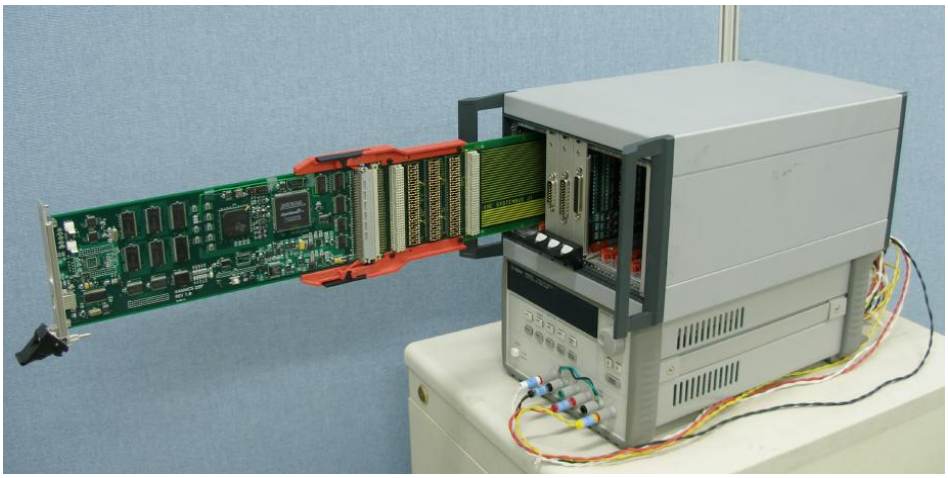

Figure 2. The controller box connected to the power supply

An IR sensor is mounted on fanout board in the detector housing. We have tested the board functions with CRC744, a 256×256 ROIC, and confirmed that the controller operates successfully. A scientific sensor for observation is ALADDIN Ⅲ Quadrant (a 512×512 InSb array, manufactured by Raytheon). Windows-based PC is used to save image

and communicate with the controller. Communication port is adopted USB 2.0 and TCP/IP interface. Correlated Double Sampling (CDS) is basically used as the readout mode.

3. HARDWARE

3.1 DSP board

The DSP board consists of floating point operational DSP (TMS320C6713 by TI), FPGA, USB interface, 384MB SDRAM and DPRAM. We download clock pattern data from the PC and save it in the DPRAM. The board has two different booting methods; emulation booting and Flash ROM booting, which is selected by jumper configuration. The DSP board exchanges addresses and data with other boards through the controller backplane. The MS Windows-based PC communicates with this board using USB 2.0 interface circuit by a speed of 14MB sec^{-1}. TCP/IP interface method is also available. We use USB to Fiber optics converter to extend the distance of USB communication. In addition, this board includes two serial interface and 16 ports for digital I/O. Digital I/O ports has been used such as a micro switch signal which detects the reference position of the filter-wheel. The PCB is implemented on 10 layers, and the dimension is 279.4×101.6 mm.

The board includes the following resources.

- TMS320C6713DSP: 225 MHz, floating-point, 256KB internal RAM
- SDRAM: mass memory, 128 MB, 32-bit interface (MT48LC32M16A2)
- FPGA: programmable “glue” logic, clock pattern generation (EP1C6Q240C8 - ALTERA)
- EEPROM: download/upload clock pattern, 64K I2C CMOS serial EEPROM (24LC64)
- Flash-ROM: 4 Mb (512KB, 8-bit interface), CMOS uniform sector 32-pin flash memory (AM29LV040B)
- USB interfaced controller: high-speed USB peripheral controller (CY7C68013)
- RS232: two-port serial interface (MAX3232)
- 4 user LEDs: writable through CPLD
- Digital I/O

Fig. 3 and Fig. 4 show the block diagram and the assembled board, respectively.

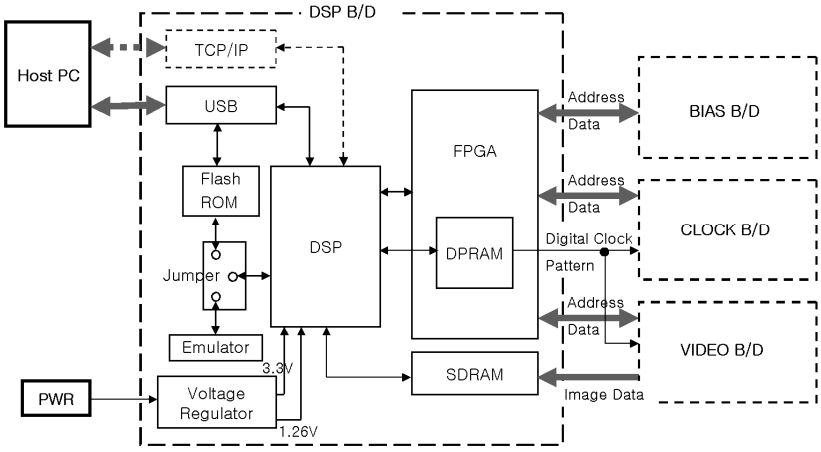

Figure 3. Block diagram of the DSP board. This board controls other boards and saves the resulting image data. It contains DSP, FPGA, SDRAM, USB, Flash ROM, and voltage regulator.

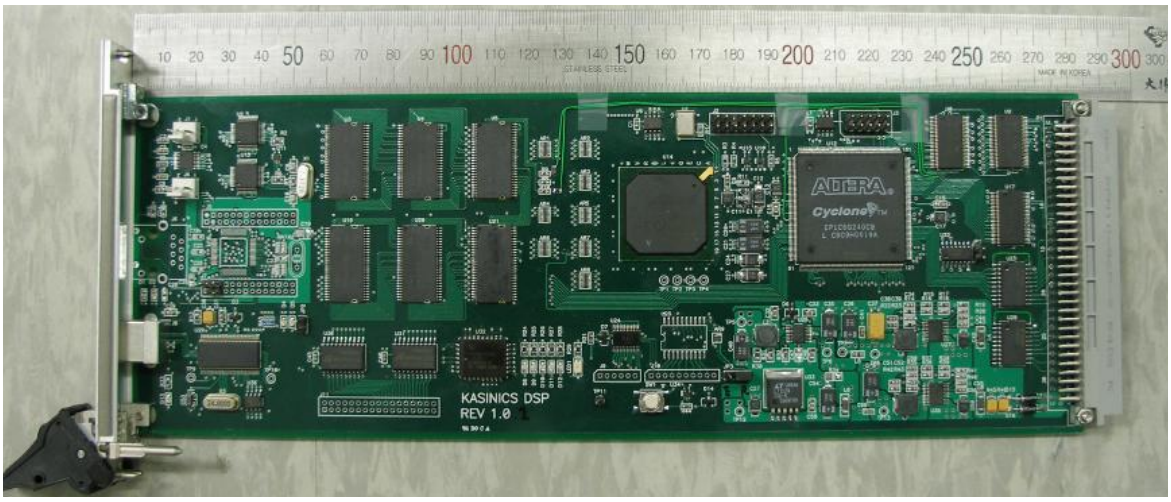

Figure 4. DSP board: 10 layers. Dimension: 279.4×101.6 mm.

Clock pattern Generator

The Clock pattern Generator circuit is on the DSP board. Clock timing is downloaded from PC and then saved on the DPRAM. Therefore the controller is able to use many kinds of readout modes and operate any type of ROIC by modification of clock pattern. FPGA (Altera, EP1C6Q240C8) is used to generate clock pattern. Digital pattern generation logic is programmed by QuartusII 5.0 software and burned to FPGA chip via Byte BlasterII. There are Reset mode and Readout mode in a clock pattern.

The Clock pattern timing table has 512 addresses each has 16-bit data and the resolution of clock timing is 500 ns for CRC744. The timing resolution and address number are able to change by user define.

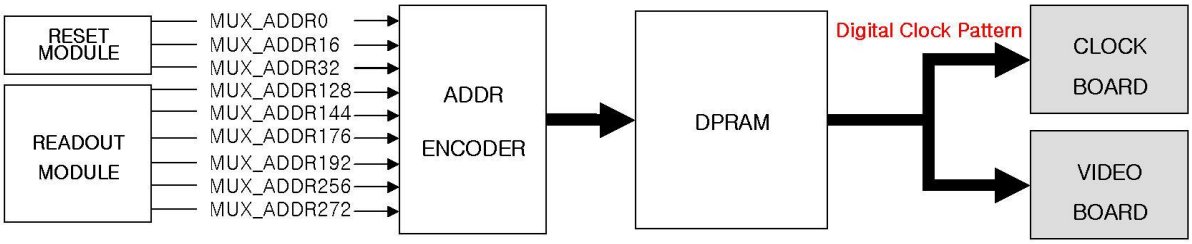

Figure 5. Clock pattern Generator. It provides 15 digital clock patterns to the Clock board and 1 pattern to the Video board.

3.2 Bias board

Since the Adjustable Bias Output is needed 12 for CRC744 ROIC and 11 for ALADDIN III Quadrant, only one Bias board is required to operation (see Fig. 6). This board has the 16-channel DAC with 0.48 mV resolution, the 8-channel ADC for monitoring voltage level, and the analog switch which controls setting voltage transmitting from the board to sensor. CPLD (EPM3256, Altera) has the address code of this board and receives command signals from DSP. And it sets DAC values through serial interface and transmits ADC values to DSP. The DAC makes 16 bias voltages by using four devices (DAC 8420, 12bit, 4 channels). This board also has the amplifier circuit for three hall sensors which are used to know absolute position of filters. A 8-channel ADC (AD7891) device and a 16-channel CMOS Analog switch (MAX306) are used to monitor DAC voltages and hall sensor signals.

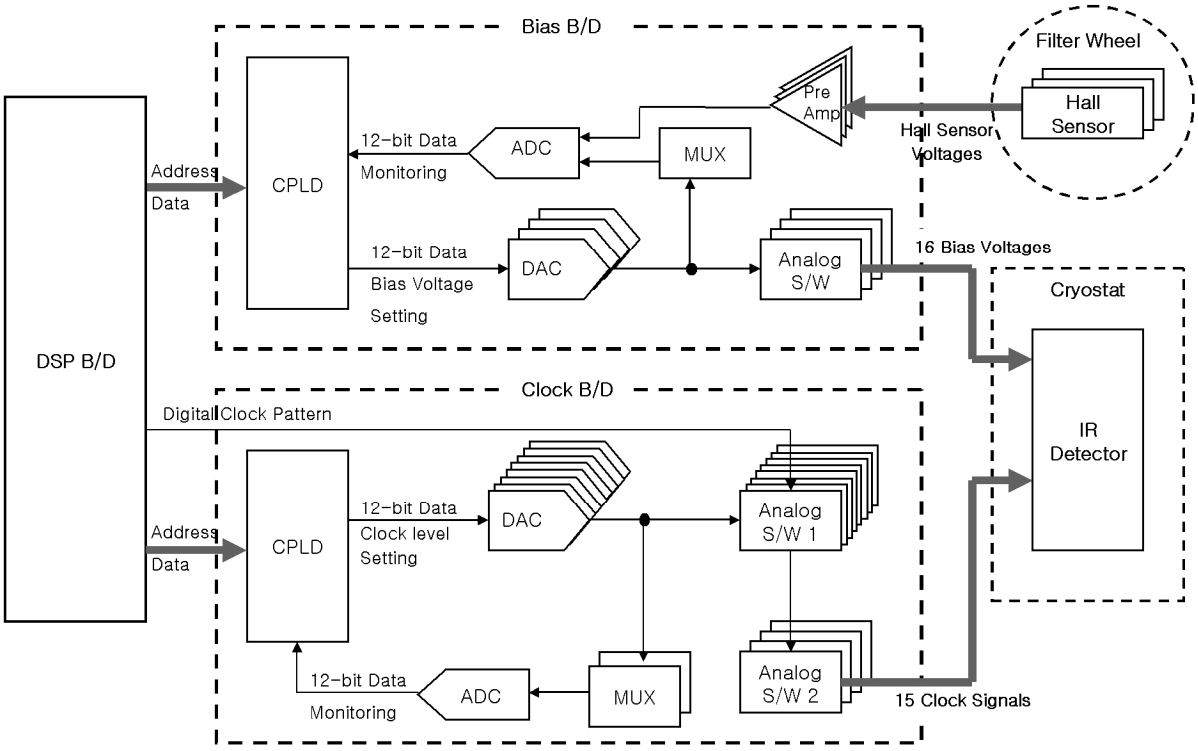

Figure 6. Block Diagram of the Bias board and Clock board.

3.3 Clock board

The Clock board generates 15 clock signals. Fig. 6 shows the block diagram of Clock board. This board uses eight 4-channel DAC (DAC8420) to generate 16 high-and-low levels. There are two MUXs and one ADC for monitoring voltage levels similarly such as Bias board. CPLD plays a role to communicate with DSP. Analog switches are used for preventing that wrong clock signals transmit to IR sensor.

3.4 Video board

The Video board consists of circuits for pre-amp, DAC and ADC for offset-voltage setting and monitoring, 16-bit ADC, and FIFO memory. The pre-amp circuit amplifies signals by 5 times and reverses signal phases. According to our simulation, the readout speed of the controller should be 10 frames sec^{-1} in order to do L-band observation at summer. For a 512×512 ALADDIN sensor, analog-to-digital conversion time should be 320 KHz at least. AD7671 as we chosen for video conversion ADC has no problem in this case. CY7C4275 is used for FIFO memory.

In case the read-noise is dominated by white noise, both linear fitting and Fowler-sampling are superior to CDS in readout methods. But in case that the read-noise of the detector is dominated by shot noise of the photons, the best signal-to-noise is theoretically achieved with CDS (Garnett et al., 1993)[3]. Linear fitting and fowler sampling need long processing times, and those are able to use for observing with long integration time. CDS, however, suits for short-time observation such as our time series photometry. But linear fitting and Fowler sampling are available for readout methods in our controller.

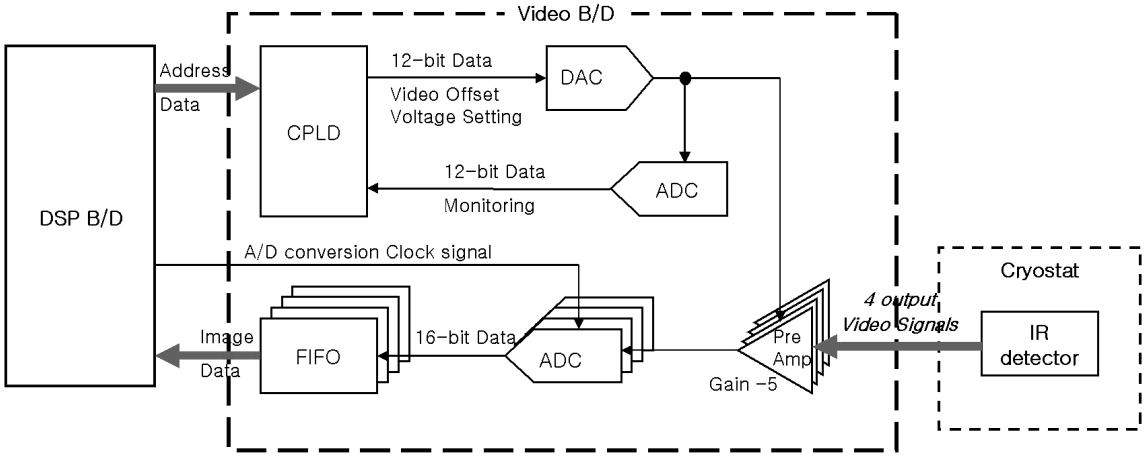

Figure 7. Block Diagram of the Video board.

This board includes the circuits for processing 4 signals. CRC744 ROIC which is used for a function test needs one Video board. In case of observation, controller needs two Video boards for readout because Aladdin III quadrant has 8 outputs. The board contains diagnostic points that confirm operation. Fig. 7 shows the block diagram of the Video board.

3.5 VME bus backplane & Packaging

The VME backplane plays a pass way to help communication between DSP board and other boards. The backplane receives power from the AC-DC linear power supply (HP E3631A) and sends it to each board with +5.4 V, +15.0 V, and -15.0V. Each board has there on power regulation circuit. Power dissipation is summarized as shown Table 1.

Table 1. Power dissipation.

Voltage	+5.4 V	+15.0 V	-15.0 V
Current	1.51 A	0.424 A	0.369 A
Power dissipation	8.154 W	6.36 W	5.535 W
Total power dissipation		20.049 W	

Backplane is J1 model made by Schroff. Its PCB (Printed Circuit Board) is implemented on 6 layers, and dimension of the plane is 3U in height and 201.8mm in width. The controller is able to contain up to 10 boards because the backplane has 10 slots. The controller enclosure is compac 3U/42HP/D312 (Schroff). It is attached on the outer panel of the cryostat.

4. FIRMWARE

Controller firmware is written in C. Windows-based compilation and linking tools, together with a source code debugger interfaced to the DSP via JTAG port, are used for code development. Executable code is stored in Flash memory, and is

able to be updated from the host PC. When the system power is on, the DSP board determines the controller configuration and the system initializes devices including DSP. In this process, the required parameters are set up in default values stored EEPROM. The voltages of the Bias and Clock board are set up in values suitable for CRC744, and memory devices such as SDRAM and FIFO are cleared.

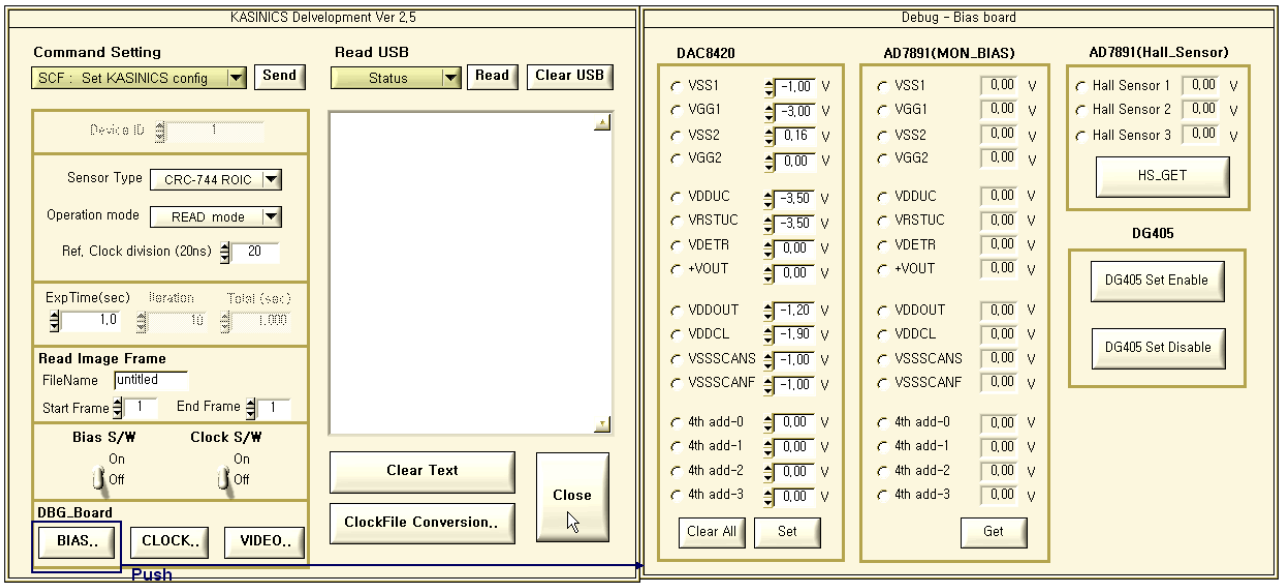

Figure 8. Left window shows main panel of the test version software. All parameters set up in this panel. Right window is debug bias board panel. We execute bias voltage setting, bias voltage & hall sensor signal monitoring, and analog switch controlling in this panel.

We developed Windows-based test version software for controller operation using CVI 6.0 tool, as shown Fig. 8. The software communicates with firmware via USB interface. The test software has functions to operate our system such as download clock pattern, set exposure time, take image frames, and send image data to PC. And it also controls Bias/Clock voltages, analog switches and monitors various voltage levels. For the observation, we are developing user friendly software based on this test software.

5. SUMMARY

We had developed IR array readout controller for the KASINICS. We had tested image acquisition in order to confirm performance of the controller in a laboratory by using test ROIC (CRC744). Test image as shown Fig. 9 was taken with standard 50mm lens attached on detector housing.

We had also acquired successfully test images from system test observation with KASINICS installed on the 61 cm telescope in SOAO. As test result, we confirmed that the controller was operated normally. And we need to optimize the controller with many kinds of test for use a 512×512 ALADDIN III Quadrant. We expect that the controller take the first light by the end of 2006.

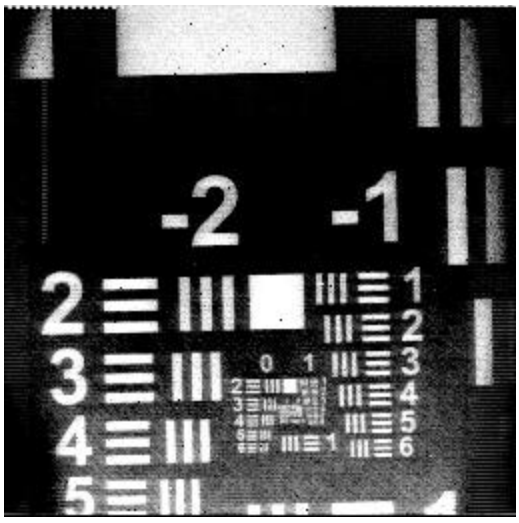

Figure 9. Test image of CRC 744.

ACKNOWLEDGMENTS

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